AMENDMENTS TO THE CLAIMS:

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1 - 5 (canceled).

6. (previously presented): A method of designing and manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the step of, in a design stage, modifying layout pattern data of said embedded array by detecting and removing a non-use area in a basic cell based on layout data of contact holes,

wherein said contact holes are for connection between an impurity region of transistors and a line thereover, said step comprising the steps of:

segmenting a pattern of said impurity region into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one or more of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

7. (original): A method according to claim 6, wherein a pattern of said impurity region includes an area corresponding with a gate, said step further comprises:

obtaining an OR pattern, as a synthesized removal pattern, between a pattern of said gate and said non-use area; and

performing said modifying by removing said synthesized removal pattern from said pattern of said impurity region.

8. (original): A method according to claim 7, wherein said modifying is performed by operating an exclusive OR between said pattern of said impurity region and said synthesized removal pattern.

9. (original): A method according to claim 6, wherein said one or more individual contact hole patterns are those in line along a direction traversing a gate pattern.

10. (original): A method according to claim 6, wherein said one or more individual contact hole patterns is one individual contact hole pattern, and an area of said removal unit excludes a close area to a gate.

11. (previously presented): A method of designing and manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the step of, in a design stage, modifying layout pattern data of said embedded array by detecting and removing a non-use area in a basic cell based on layout data of contact holes,

wherein said contact holes are for connection between an impurity region and a line thereover having a substrate bias potential, said step comprising the steps of:

segmenting a pattern of said impurity region into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

12. (previously presented): A method of designing and manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the step of, in a design stage, modifying layout pattern data of said embedded array by detecting and removing a non-use area in a basic cell based on layout data of contact holes,

wherein said contact holes are for connection between a gate of a transistor and a line thereover, said step comprising the steps of:

segmenting a pattern of said gate into individual segmentation patterns each as a removal unit, each segmentation pattern corresponding with one of all individual contact hole patterns that can be arranged; and

judging one of said removal units as said non-use area if an individual contact hole pattern corresponding with said one of said removal unit is not existent.

13. (original): A method according to claim 12, wherein said individual segmentation patterns have one that is a member of a single transistor assumed to exist; and judging said one of said individual segmentation patterns as said non-use area if said single transistor is not existent.

14 - 16 (canceled).

17. (Previously presented) A method of designing and manufacturing a semiconductor integrated circuit having an embedded array, said embedded array having basic cells arranged in a matrix, said method comprising the step of, in a design stage, modifying layout pattern data of said embedded array by detecting and removing a non-use area in a basic cell based on layout data which represents that a contact hole is not existent.